Fig. 1(A)

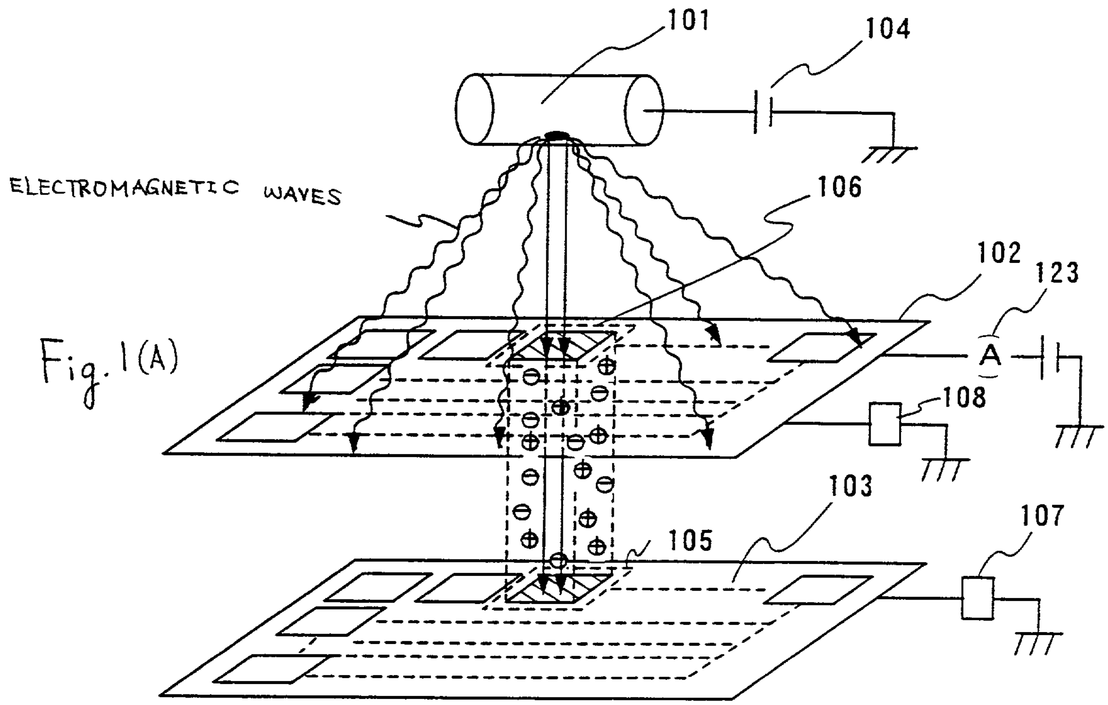


Fig. 1(B)
ENLARGED DIAGRAM OF 105

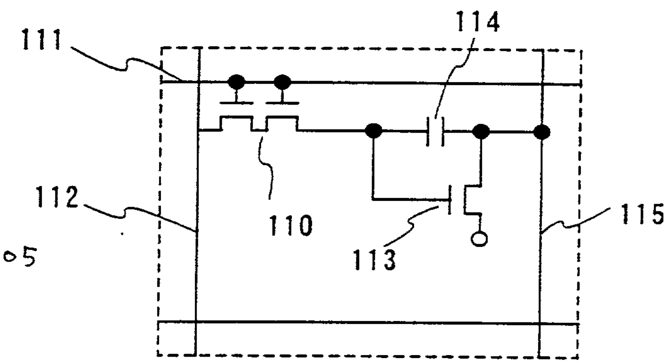
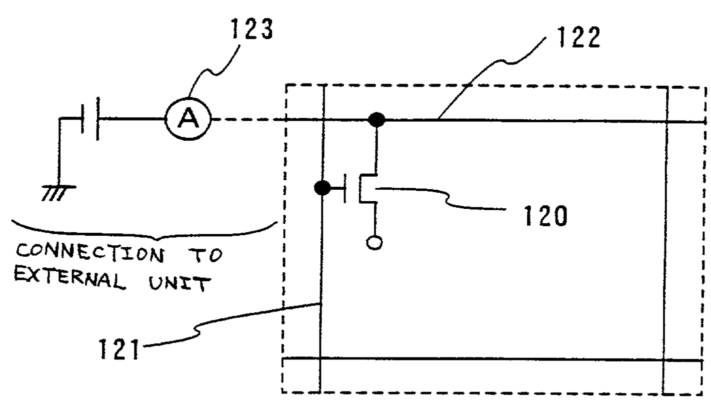


Fig. 1(C)
ENLARGED DIAGRAM OF 106



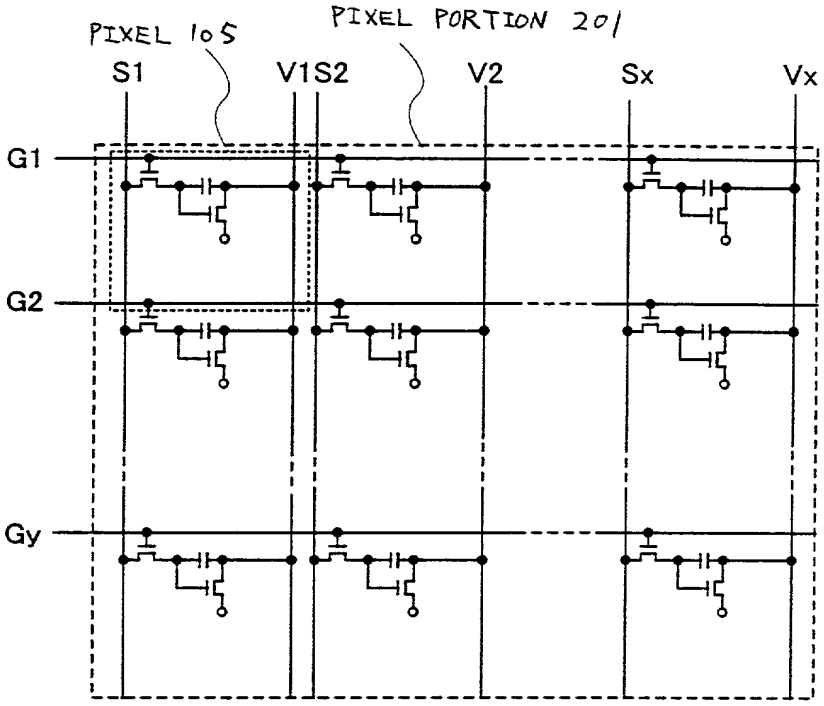

PIXEL 105
PIXEL PORTION 201
S1
V1
S2
V2
Sx
Vx
G1
G2
Gy

Fig. 2(A)

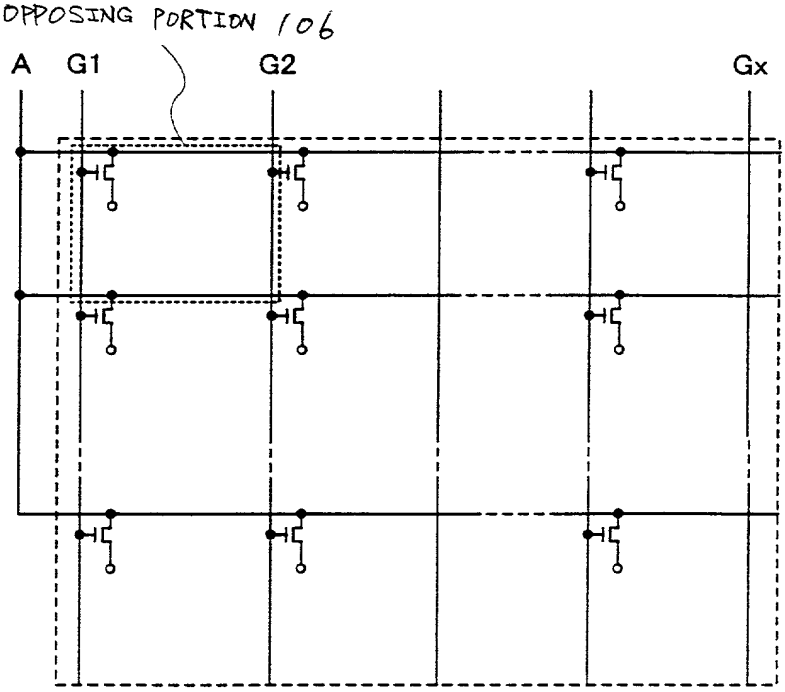

OPPOSING PORTION 106
A
G1
G2
Gx

Fig. 2(B)

Fig. 3(A)

(1, 1)	(2, 1)	(3, 1)	(4, 1)		(x-1, 1)	(x, 1)
(1, 2)	(2, 2)	(3, 2)	(4, 2)		(x-1, 2)	(x, 2)
(1, 3)	(2, 3)	(3, 3)	(4, 3)		(x-1, 3)	(x, 3)
(1, 4)	(2, 4)	(3, 4)	(4, 4)		(x-1, 4)	(x, 4)
(1, y-1)	(2, y-1)	(3, y-1)	(4, y-1)		(x-1, y-1)	(x, y-1)
(1, y)	(2, y)	(3, y)	(4, y)		(x-1, y)	(x, y)

Fig. 3(B)

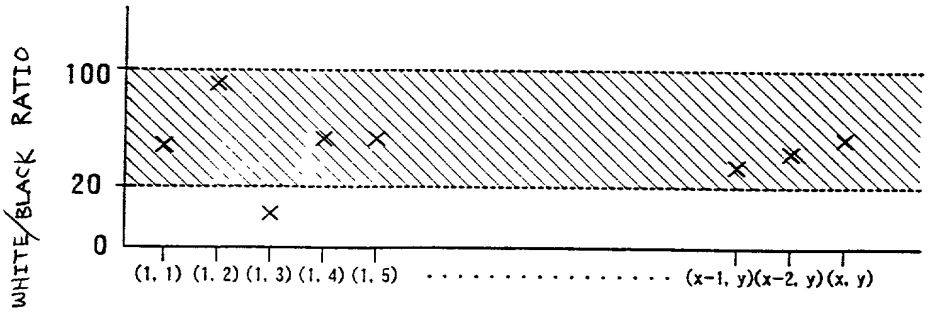


Fig.4(A) FORMATION OF ISLAND SEMICONDUCTOR LAYER, GATE-INSULATING FILM, AND FIRST AND SECOND CONDUCTING FILMS FOR GATE ELECTRODES

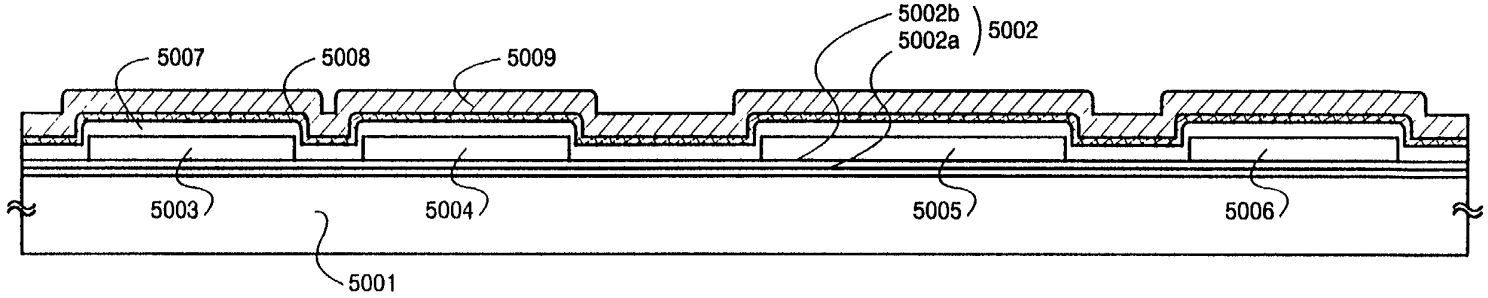


Fig.4(B) FIRST ETCHING AND FIRST DOPING

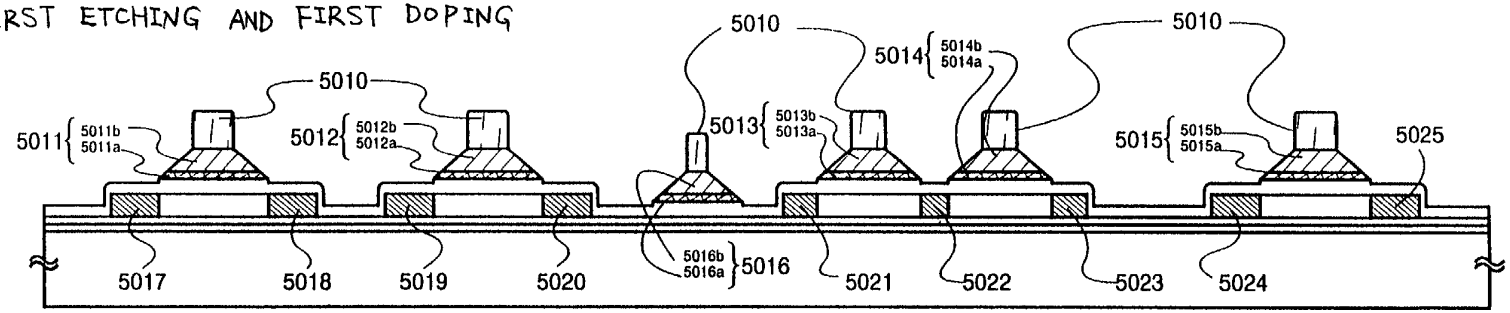


Fig.4(C) SECOND ETCHING

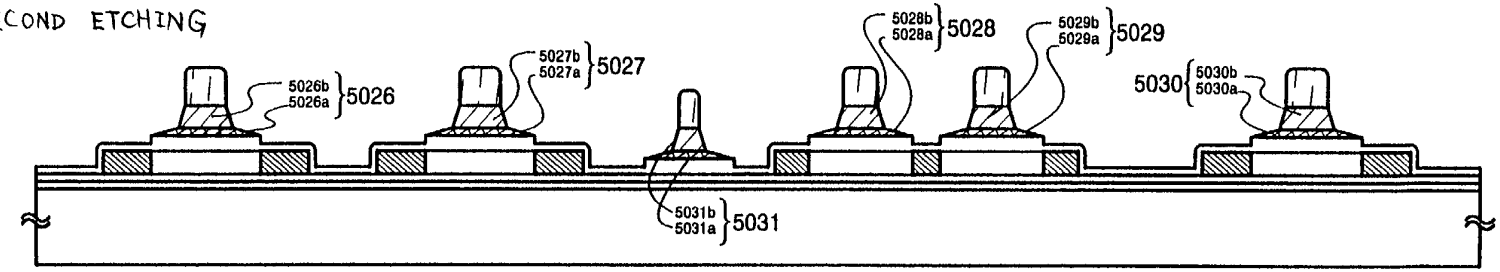


Fig.5(A) SECOND DOPING

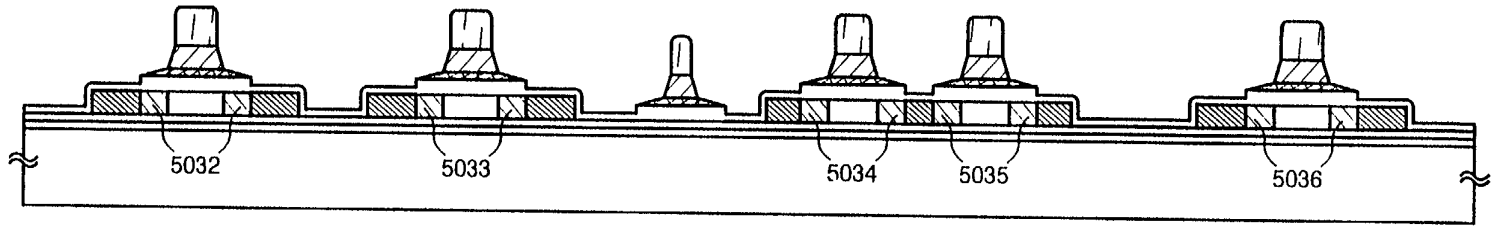


Fig.5(B) THIRD ETCHING

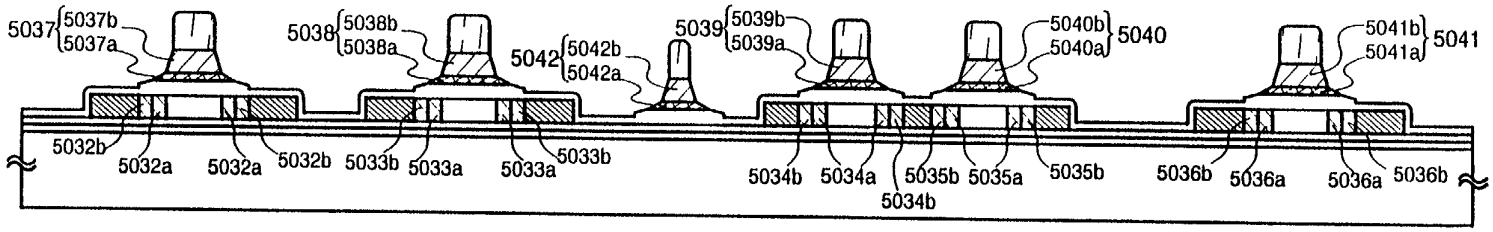


Fig.5(C) THIRD DOPING

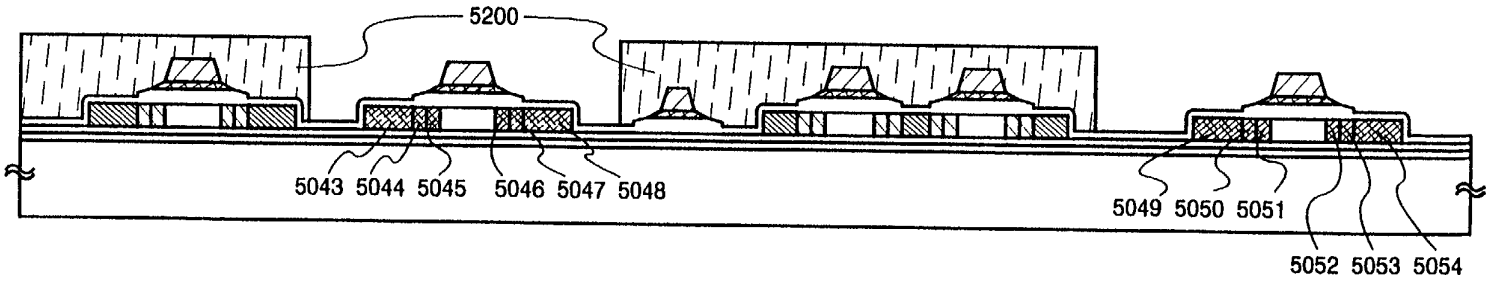


Fig. 6(A) FORMATION OF THE FIRST AND SECOND INTERLAYER-INSULATING FILMS, WIRINGS AND PIXEL ELECTRODES

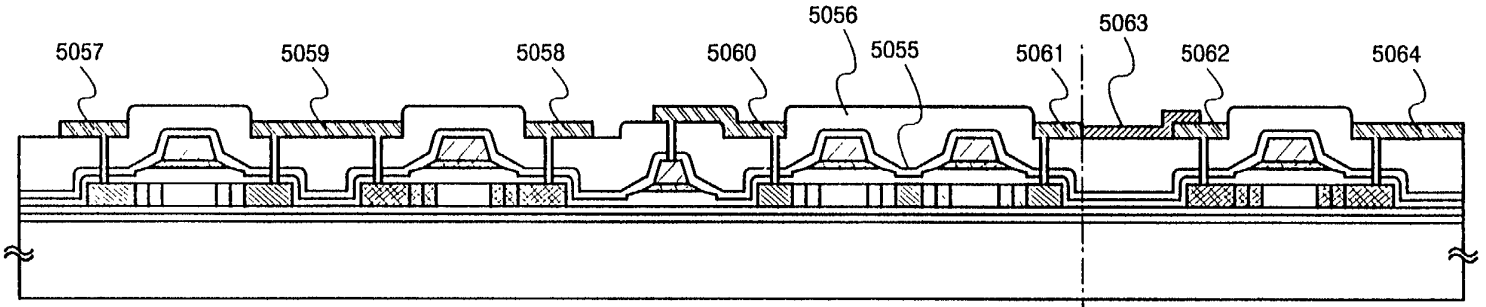
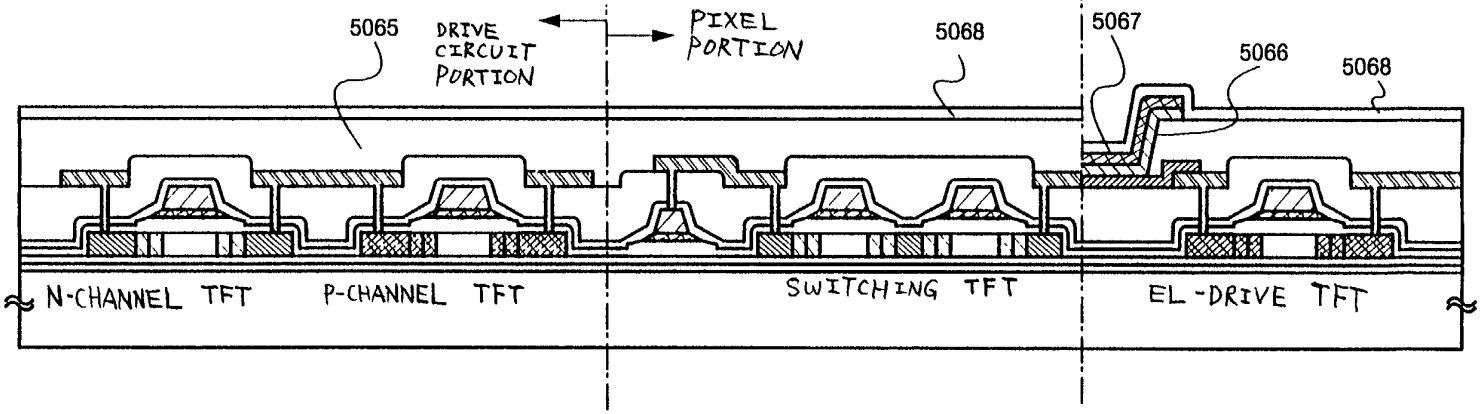


Fig. 6(B) FORMATION OF THE THIRD INTERLAYER-INSULATING FILM, EL LAYER, CATHODES AND PASSIVATION FILM



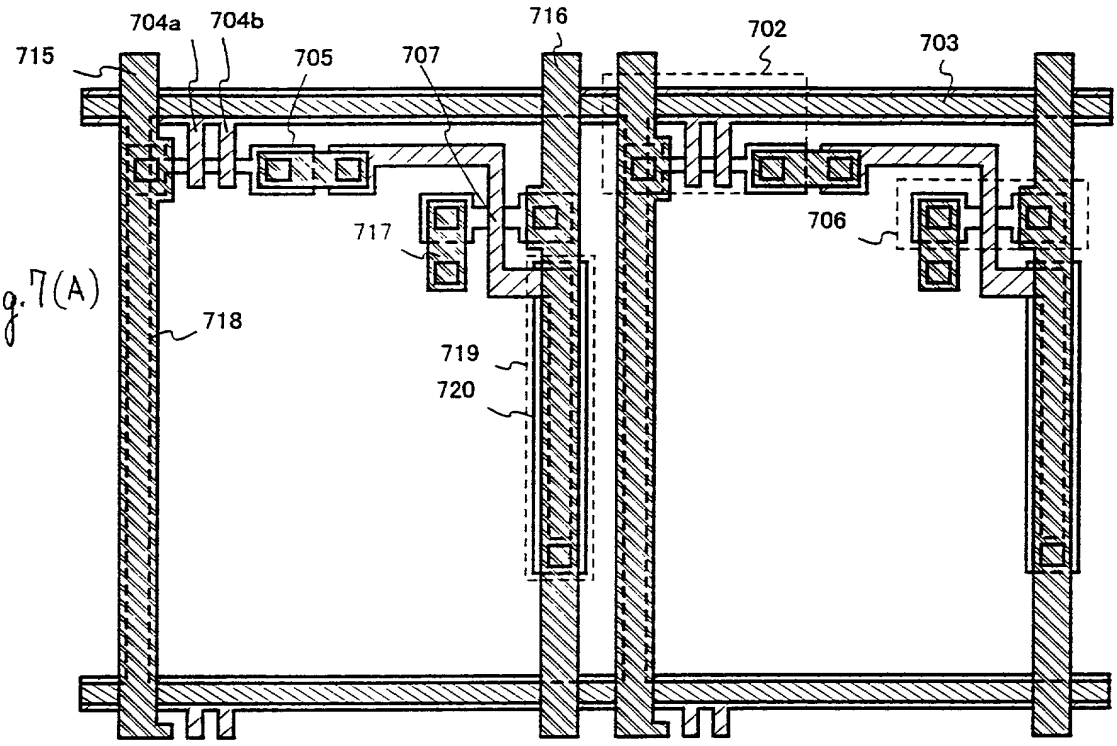

704a
704b
716
715
705
707
702
703
717
706
718
719
720

Fig. 7(A)

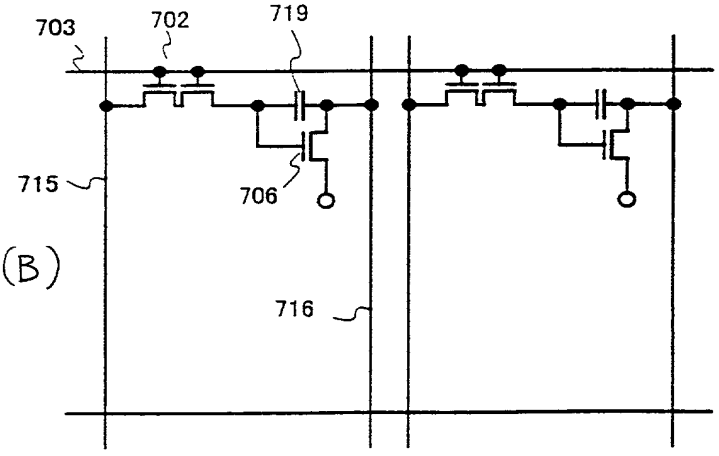

703
702
719
715
706
716

Fig. 7(B)

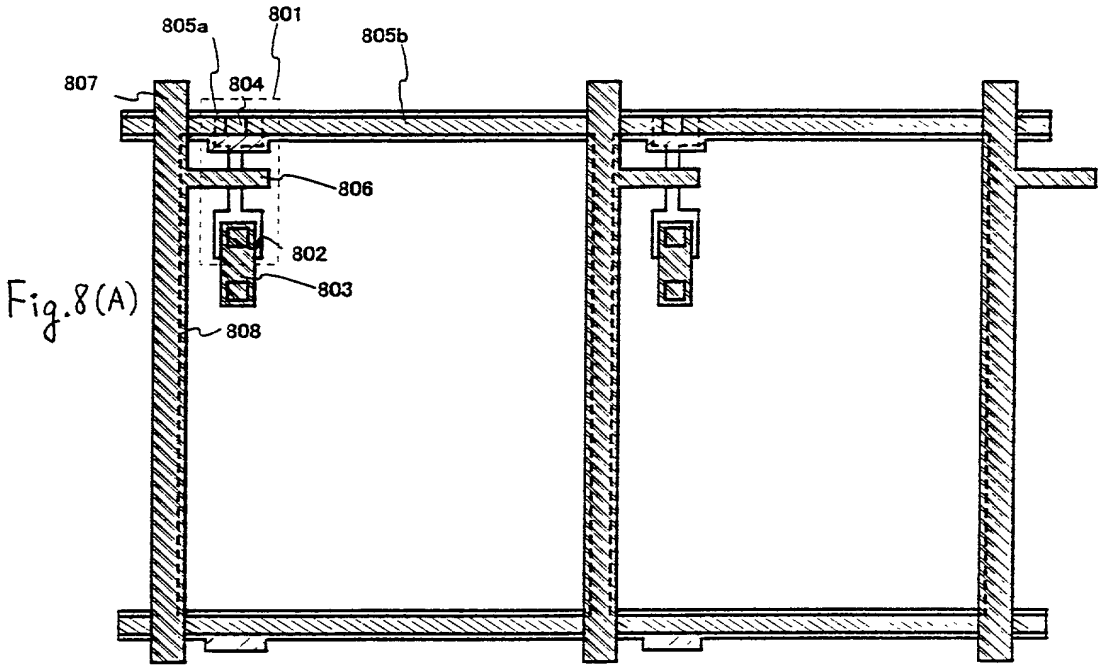


Fig.8(A)

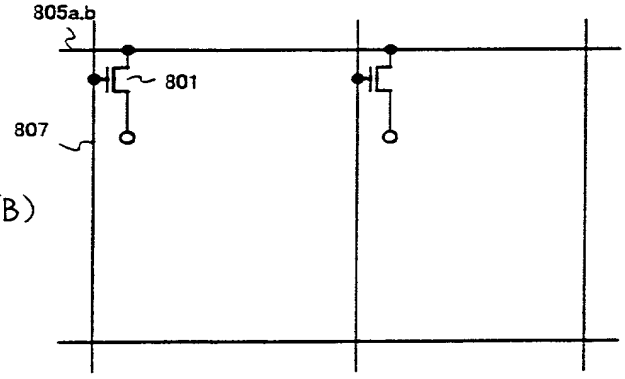


Fig.8(B)

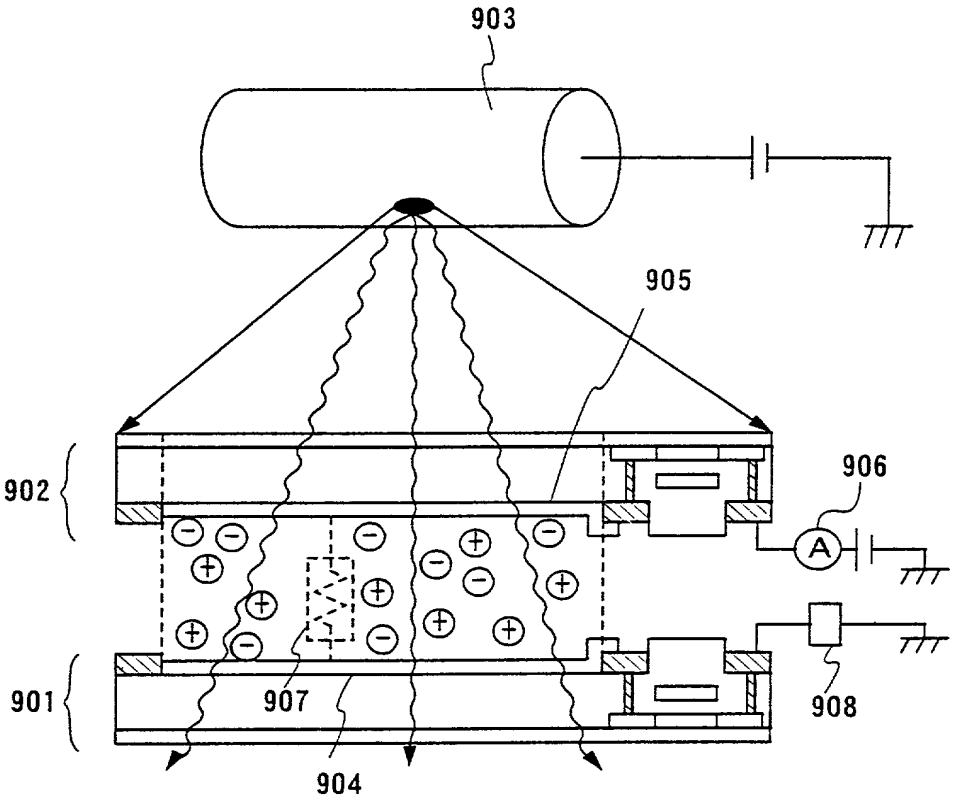


Fig. 9

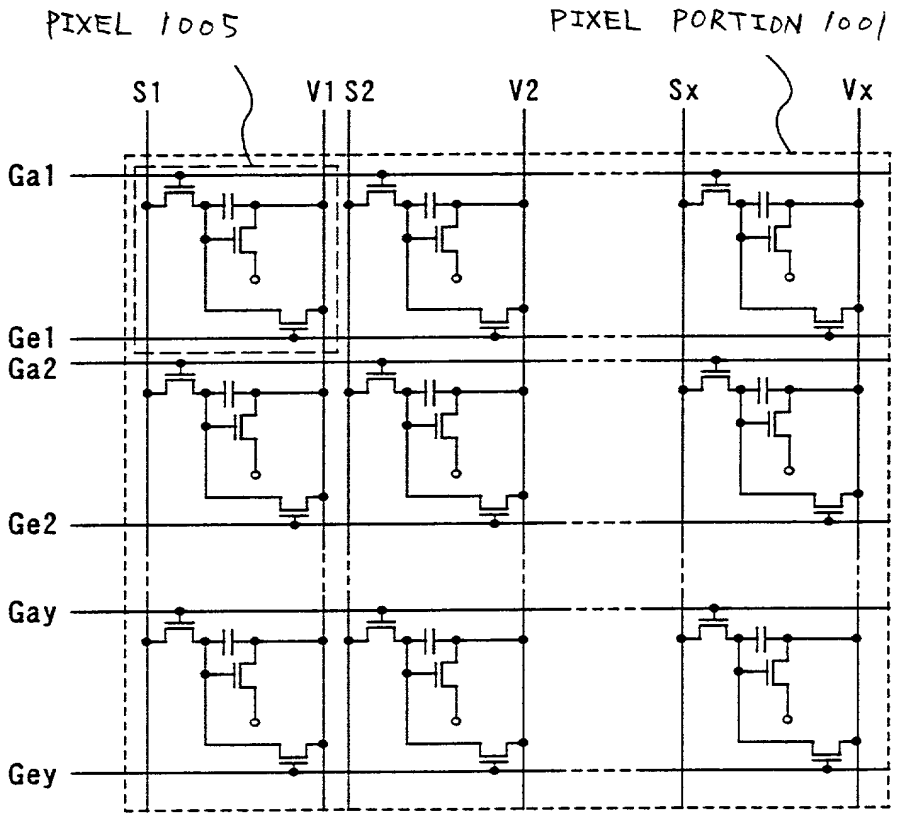

PIXEL 1005
PIXEL PORTION 1001
S1
V1
S2
V2
Sx
Vx
Ga1
Ge1
Ga2
Ge2
Gay
Gey

Fig. 10

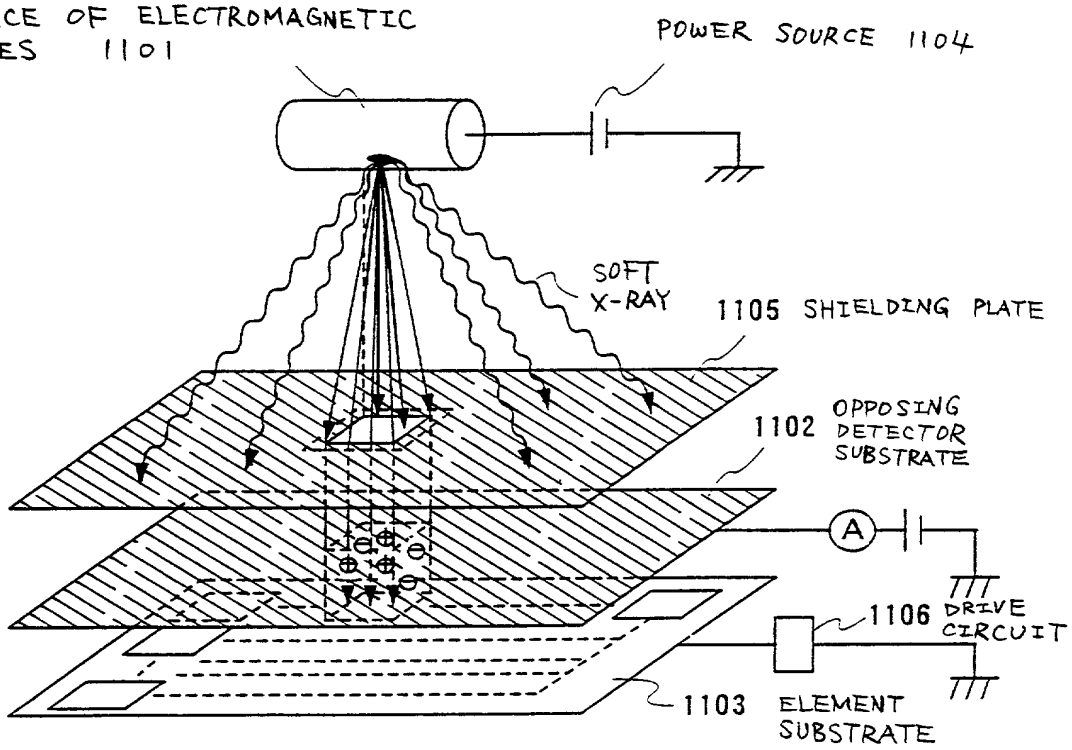

SOURCE OF ELECTROMAGNETIC WAVES 1101
POWER SOURCE 1104
SOFT X-RAY
1105 SHIELDING PLATE
1102 OPPOSING DETECTOR SUBSTRATE
A
1106 DRIVE CIRCUIT
1103 ELEMENT SUBSTRATE

Fig. 11

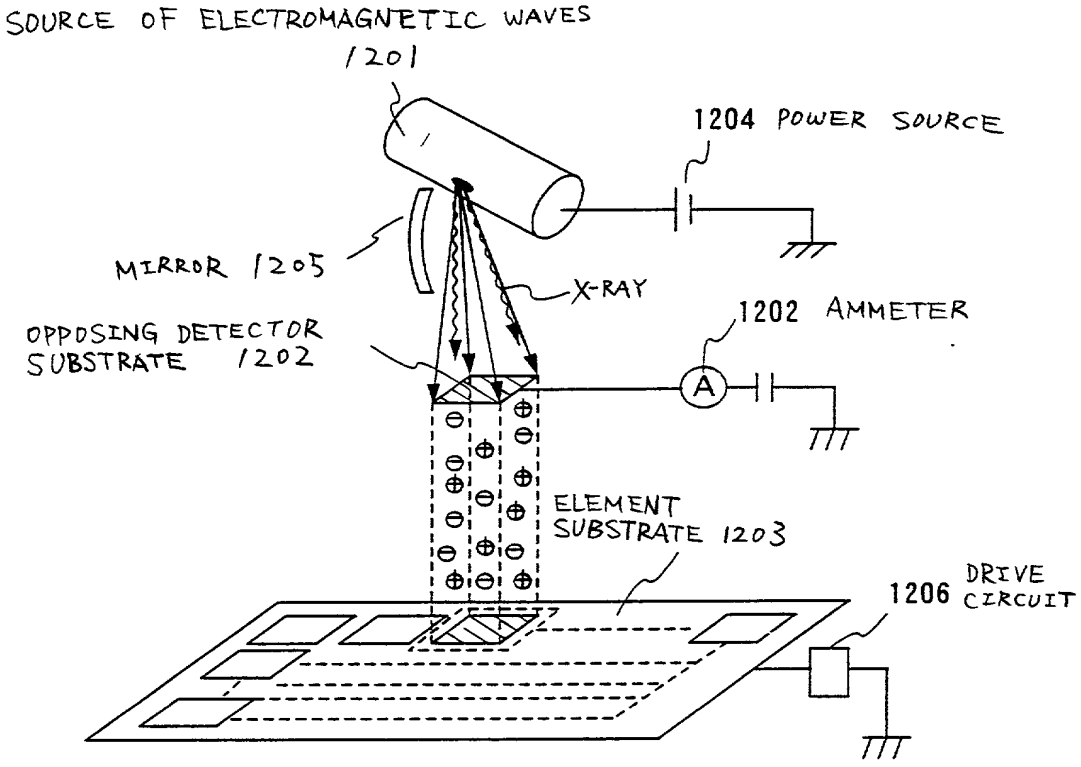
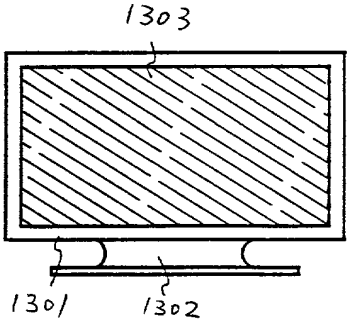

SOURCE OF ELECTROMAGNETIC WAVES
1201
1204 POWER SOURCE
MIRROR 1205
X-RAY
1202 AMMETER
OPPOSING DETECTOR SUBSTRATE 1202
A
ELEMENT SUBSTRATE 1203
1206 DRIVE CIRCUIT

Fig. 12

Fig.13(A)



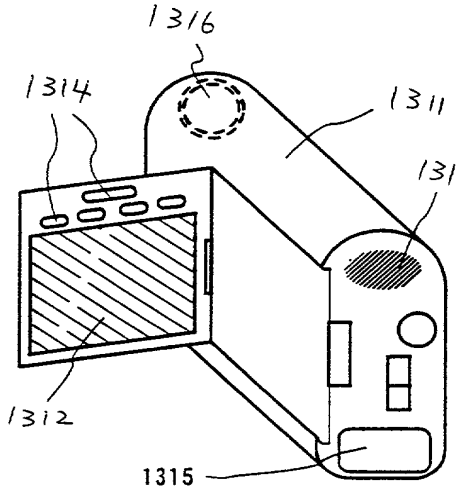


Fig.13(B)

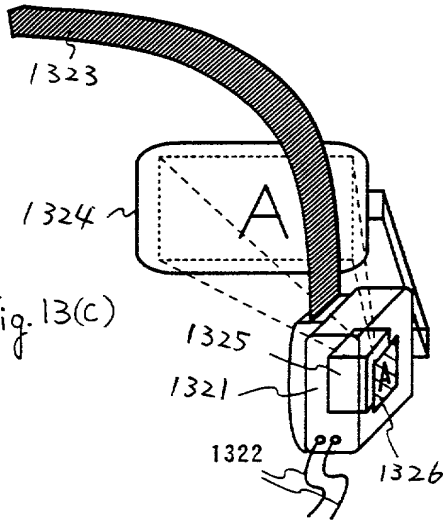


Fig.13(C)

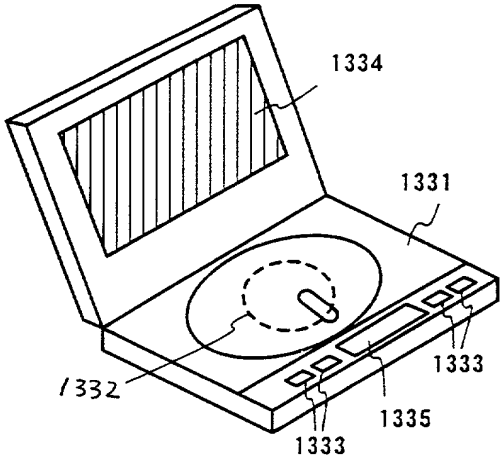


Fig.13(D)

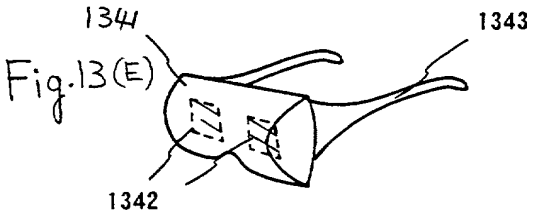


Fig.13(E)

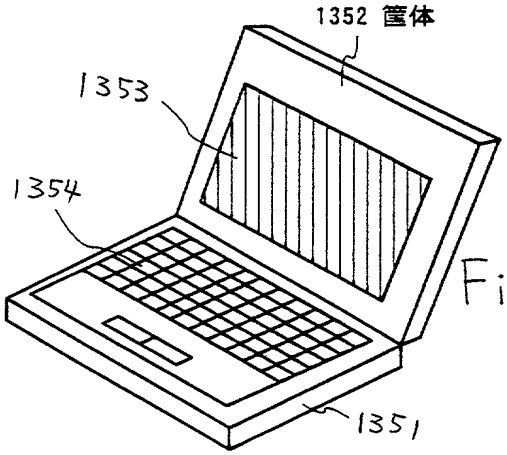


Fig.13(F)

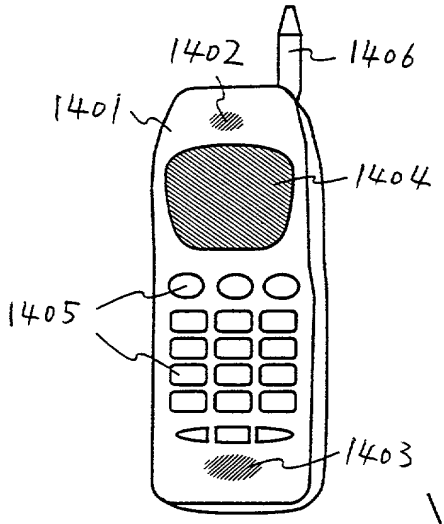


Fig. 14 (A)

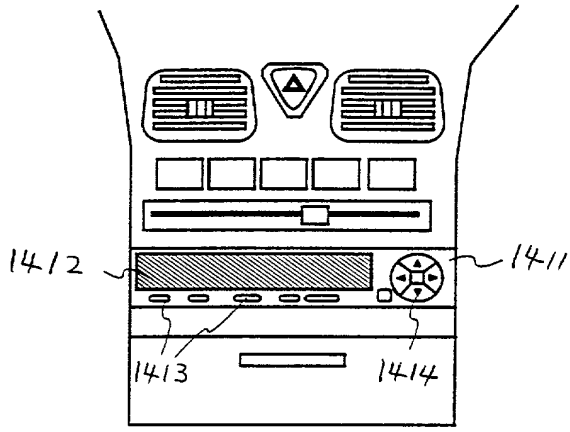


Fig. 14 (B)

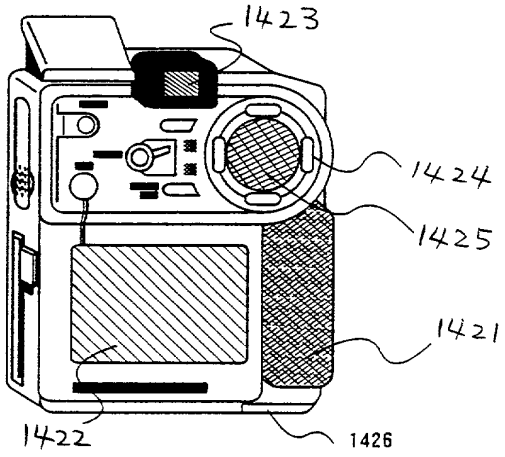


Fig. 14(C)

Fig. 15

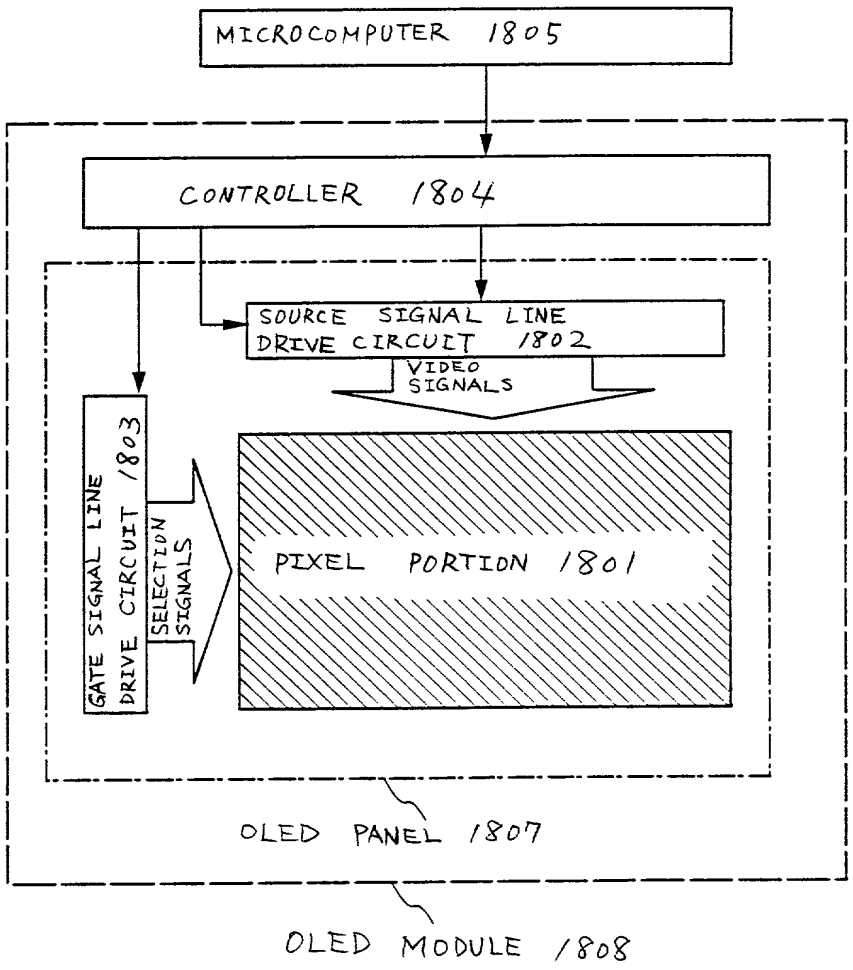

MICROCOMPUTER 1805
CONTROLLER 1804
SOURCE SIGNAL LINE DRIVE CIRCUIT 1802
VIDEO SIGNALS
GATE SIGNAL LINE DRIVE CIRCUIT 1803
SELECTION SIGNALS
PIXEL PORTION 1801
OLED PANEL 1807
OLED MODULE 1808

Fig. 16(A)

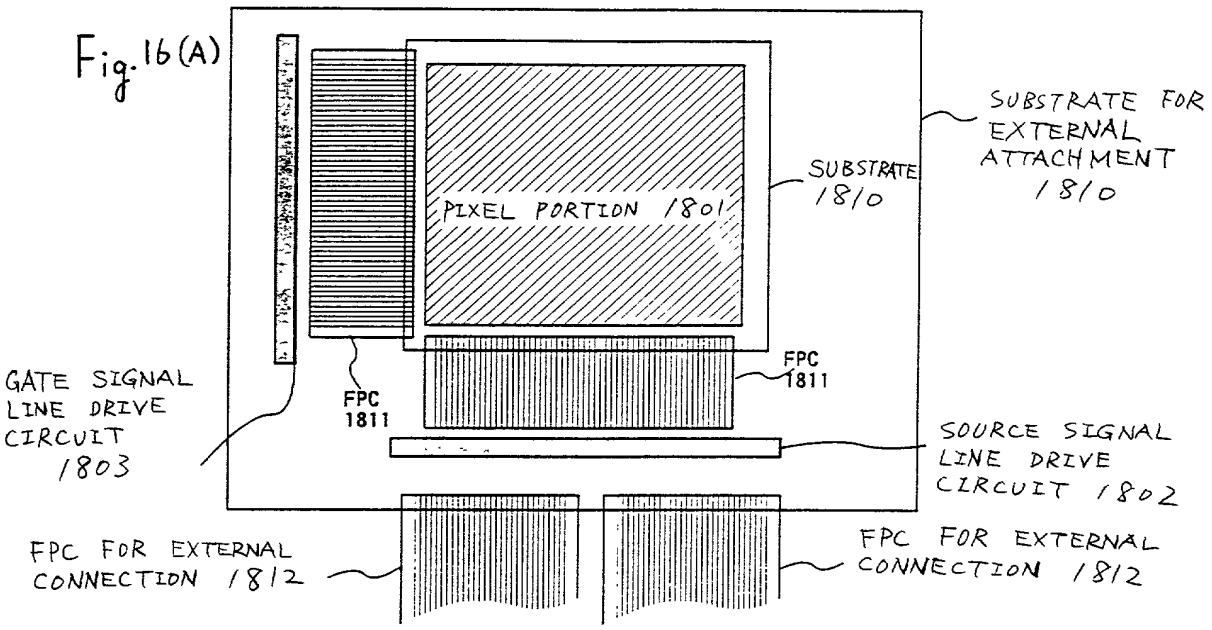


Fig. 16(B)